**Hardik J Patel EEC 180A**

**Lab 5 Report – Counter Design**

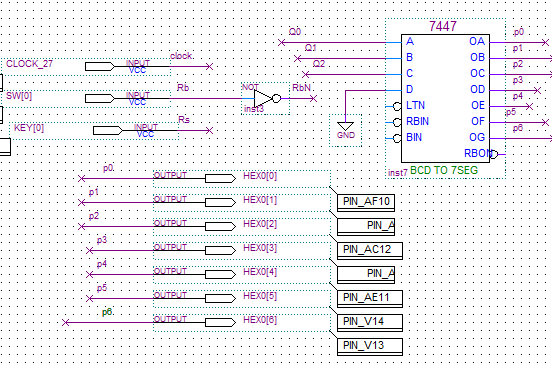
**Objective**

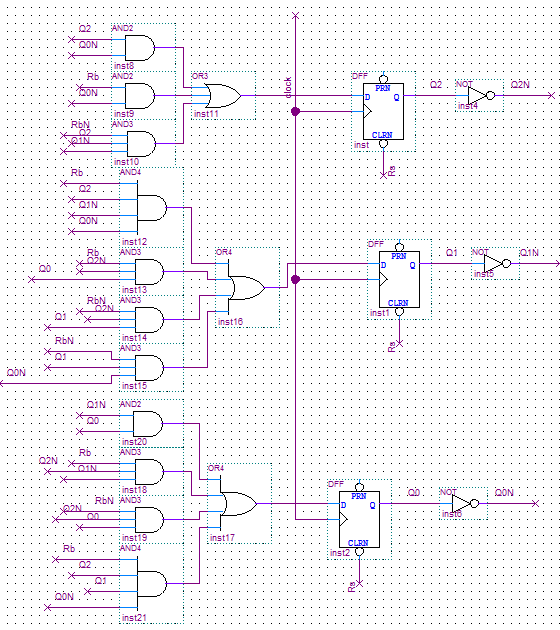
The purpose of this lab was to design a counter, using available gates and flip-flops, which counted in a desired sequence given to us. This was done by deriving the input equations for the D flip-flops using a state table and K-maps. Also, this lab helped understand the working differences between the Moore FSM and the Mealy FSM.

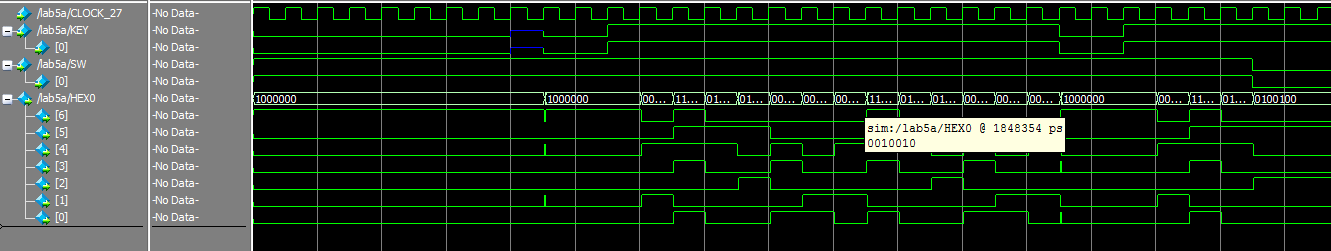
**Design and Test Procedure**

The design of this counter was completed in the pre-lab. The specific counter sequence was given and it was used to created and complete a state transition table using D flip-flops. Once the table was completed, the next state columns were used to fill k-maps for each and find the minimum sum pf product equations for each input signal to the D flip-flops. Using the SOP equations the design was implemented on Quartus II. Since 27 MHz is a very fast frequency for the eyes, a counter was used from the Quartus II library too verify on the DE2 board. Once the design was verified, the design was loaded on the ModelSim-Altera program to study and understand the waveforms. As in previous labs the, HEX1-HEX7 were turned off by connecting them to VCC.

**Schematic of the counter:**

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**ModelSim-Altera Simulation:**

The Mealy FSM design for this counter also incorporates the original input Rb into the output. But since this is a counter and we cannot miss a number in the series, the input Rb will not have an impact on the counter.

**Results and Answers to Questions**

Q. Compare Design I and Design II of the sequential circuit. Describe any advantages or disadvantages of the Moore design for this circuit.

Ans. The Moore has the advantage of less number of gates. To incorporate Rb into the final combinational logic for the output, we will need to use an extra gate. Hence, Moore is cost effective. Mealy has the advantage of skipping a step if not needed, but in this counter this is not possible as no number can be skipped.

Q. A third design for the counter circuit might use a Moore machine where the state bits were not used as the outputs. For example, the state bits might be the binary count sequence 0 – 6. How would this design would with Designs I and II (assuming your assigned count was not the straight binary count sequence 1 to 6)? Which design is likely to require the fewest gates? Justify your answer.

Ans. This design will use the most number of gates and will be the most ineffective of the three designs. This is because we will need to use a combinational logic design before the output getting the desired sequence. This will make use of many more gates, making this an ineffective design.

**Conclusions**

In this lab we learnt the implementation of a Moore and Mealy FSM and also learnt how to implement a desired sequential counter.